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Product Specification

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2008/09/24	All	First Edition for Customer		
0.2 2008/11/03	5	Resolution 1024*576	Resolution 1024*600	
	5	Pixel Pitch: 0.2175 (H) x 0.2175 (V)	Pixel Pitch: 0.2175 (H) x 0.2088 (V)	
	30		Update Shipping label	
	32-35		Update EDID	
	11		Update Functional Block Diagram	
0.3 2008/11/27	15		Update Backlight unit	
	19 & 26	Pin 36: LED_EN 3V input	Pin 36: LED_EN 3.3V input	
	32		Update carton package	
0.4 2008/12/01	33-36		Update EDID for resolution 1024*600	
0.5 2008/12/31	15		Corrcr description of LED power calculation → Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) x I_F (Normal Distribution) / Efficiency	
0.5 2008/12/31	5		Power Consumption (typ) → Correct: Power Consumption (max) -- For BLACK pattern power	



1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



Product Specification

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2. General Description

B101AW02 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 1024(H) x 600(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B101AW02 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	255.54(W")			
Active Area	[mm]	222.72(H) X 125.28(V)			
Pixels H x V		1024x3(RGB) x 600			
Pixel Pitch	[mm]	0.2175 (H) x 0.2088 (V)			
Pixel Arrangement		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance Note: I _{LED} is LED current	[cd/m ²]	180 typ (Note1)			
Luminance Uniformity (5P)		1.25 max			
Contrast Ratio		400 typ			
Response Time	[ms]	16 typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption (max)	[Watt]	2.36 @ Black Pattern			
Weight	[Grams]	170 max.			
Physical Size (w/ bracket & PCBA)	[mm]		L	W	T
		Max	243.5	147.0	3.6
		Typical	243.0	146.5	
	Min	242.5	145.0	-	
Electrical Interface		1 channel LVDS			
Surface Treatment		Glare			



Product Specification

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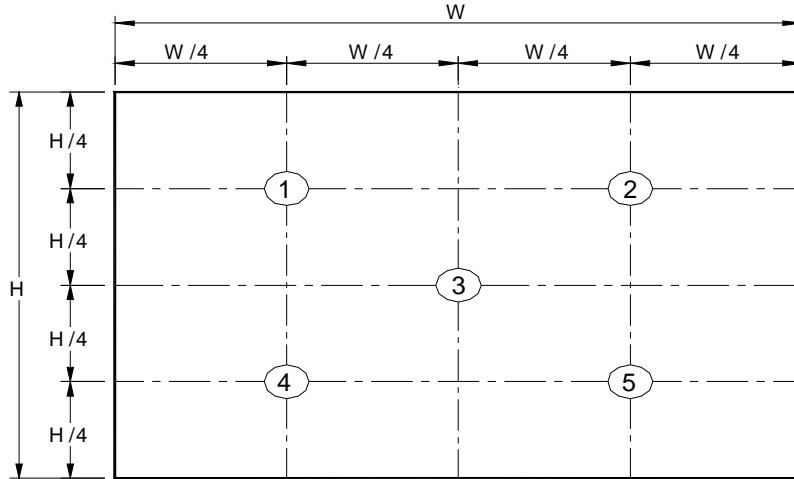
Glass thickness	mm	0.5mm
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

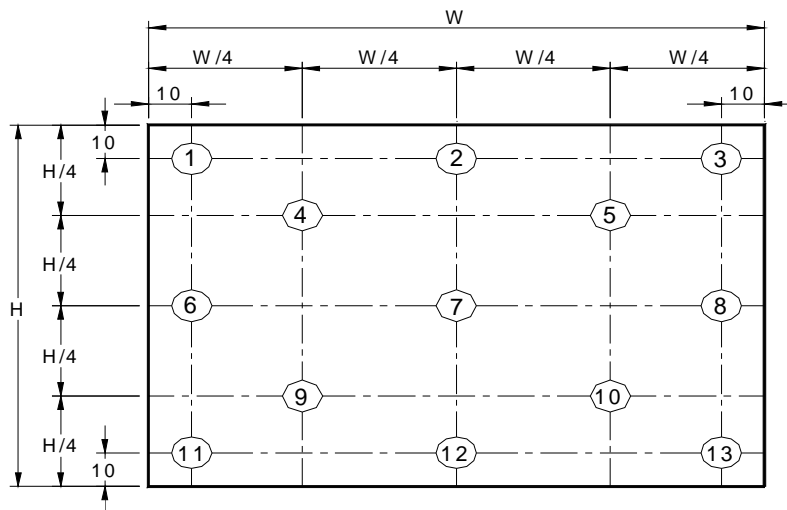
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m ²]	5 point		180	-	1,3
Viewing Angle	[degree]	Horizontal (Right)	-	45	-	3,8
	[degree]	CR = 10 (Left)	-	45	-	
	[degree]	Vertical (Upper)	-	15	-	
	[degree]	CR = 10 (Lower)	-	35	-	
Luminance Uniformity		5 Points	-	-	1.25	1,4,5
Luminance Uniformity		13 Points	-	-	1.6	2,4,5
CR: Contrast Ratio			300	400	-	5,7
Cross talk	%				4	4,6
Response Time	[msec]	Rising	-	TBD	TBD	4,7
	[msec]	Falling	-	TBD	TBD	
	[msec]	Rising + Falling	-	16		
Chromaticity of color Coordinates (CIE 1931)		Red x		TBD		4,8
		Red y		TBD		
		Green x		TBD		
		Green y		TBD		
		Blue x		TBD		
		Blue y		TBD		
		White x	0.263	0.313	0.363	
		White y	0.279	0.329	0.379	

Note 1 : 5 points position (Ref: Active area)



Note 2. 13 points position (Ref: Active area)



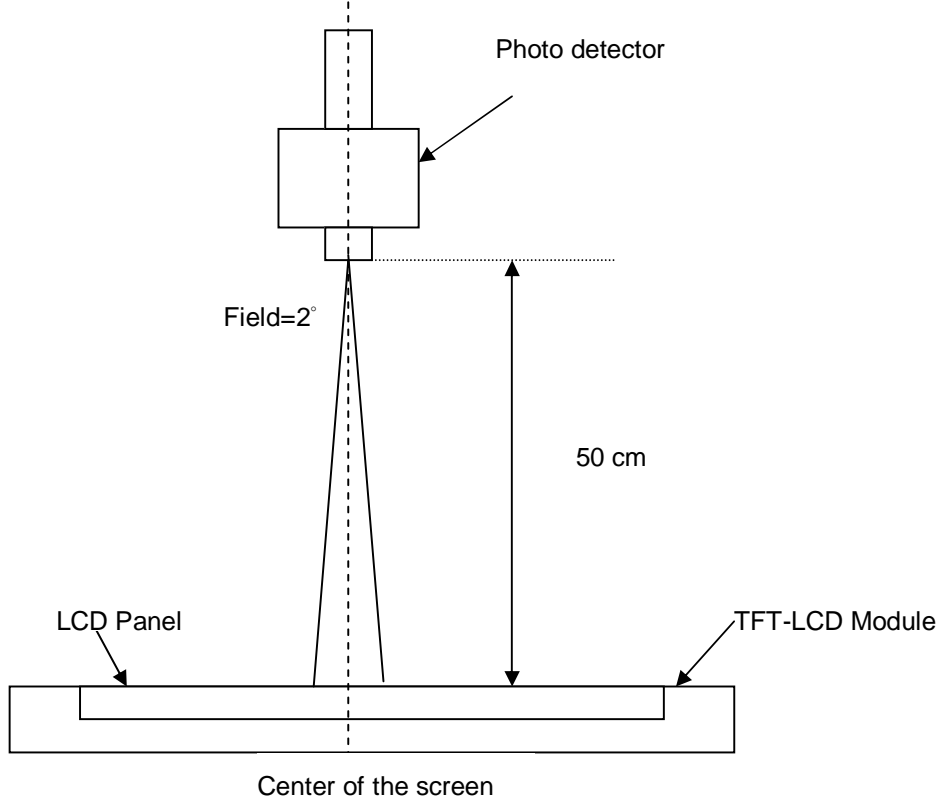
Note 3: The luminance uniformity of 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the 'White' state}}{\text{Brightness on the 'Black' state}}$$

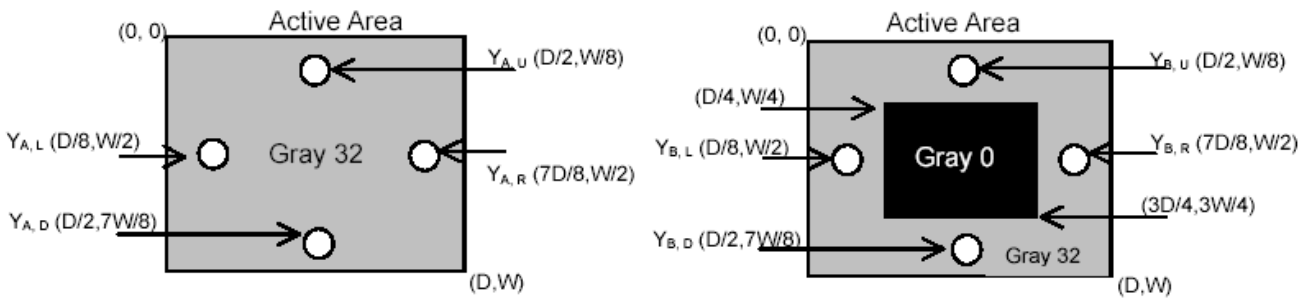
Note 6 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

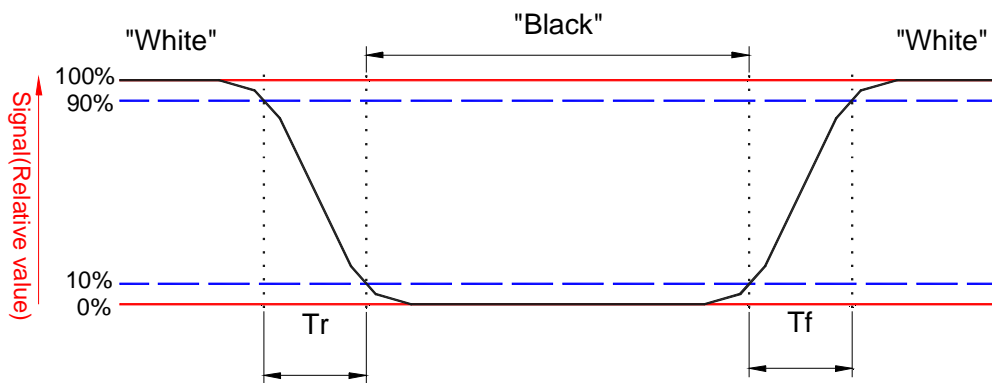
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



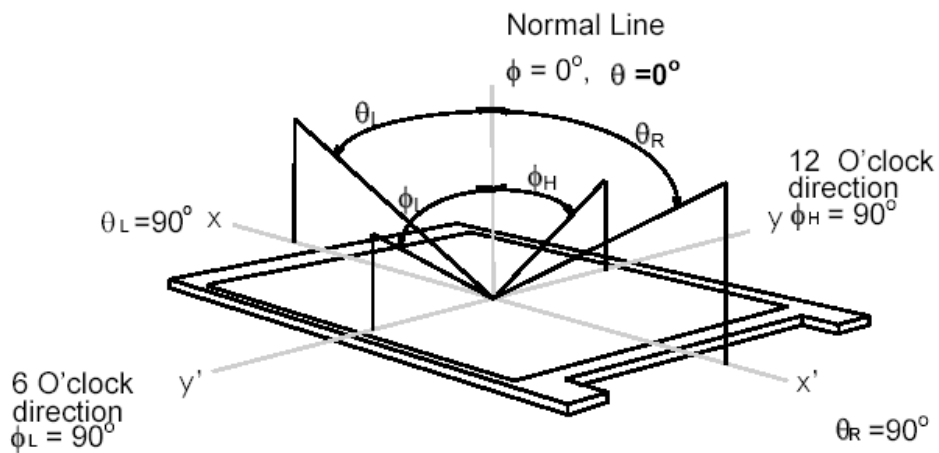
Note 7: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



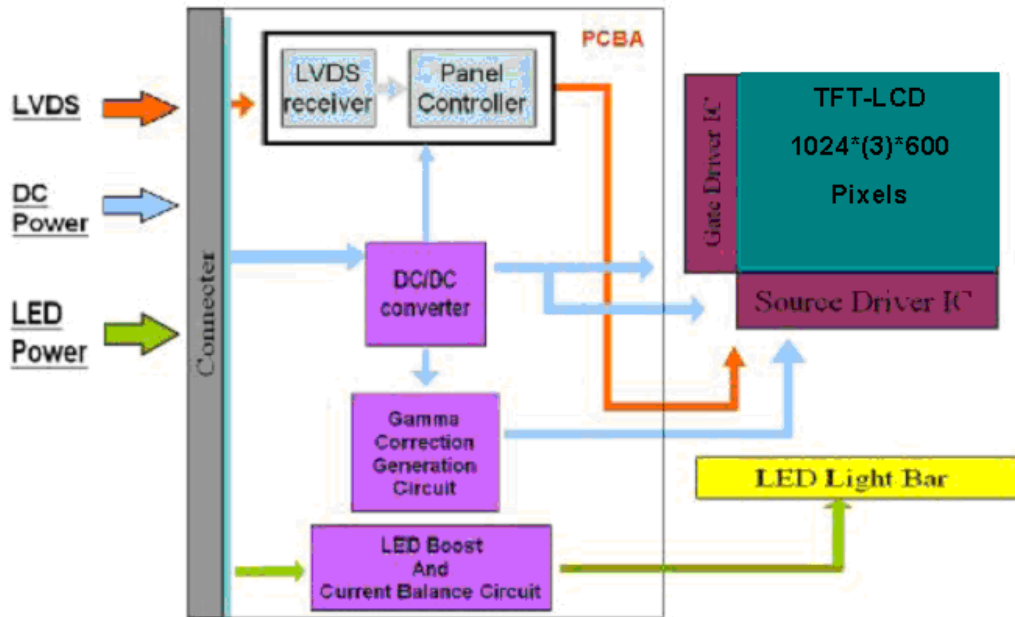
Note 8. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 170° horizontal and 170° vertical range (off-normal viewing angles). The 170° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 40 Pin (One ch/connector Module).



4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

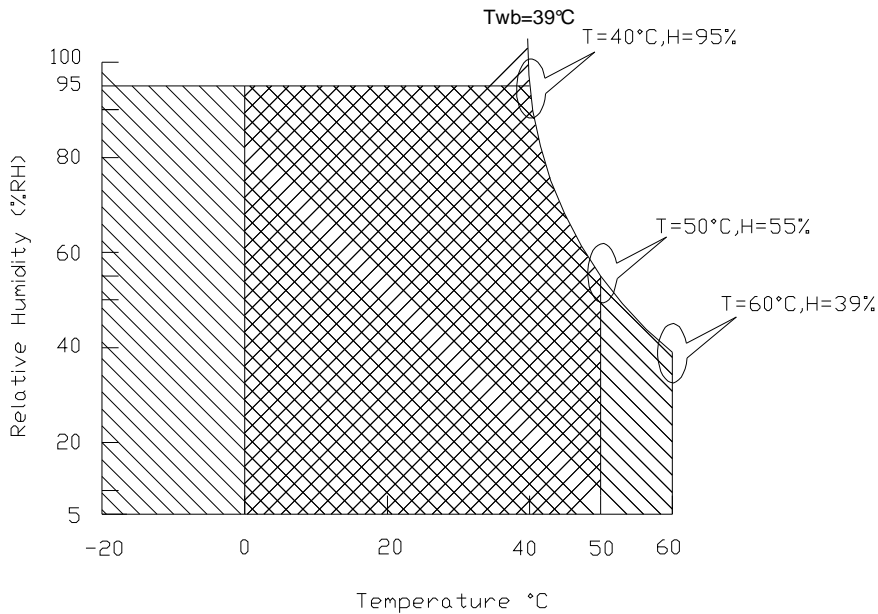
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	10	90	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	10	90	[%RH]	Note 4

Note 1: At Ta (25°C)


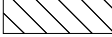
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

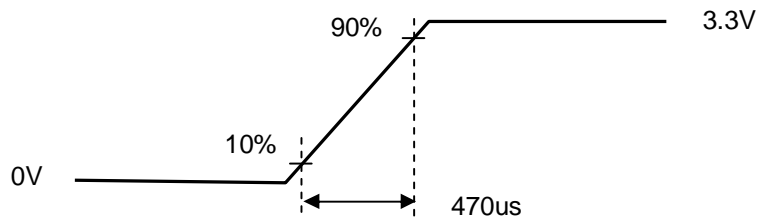
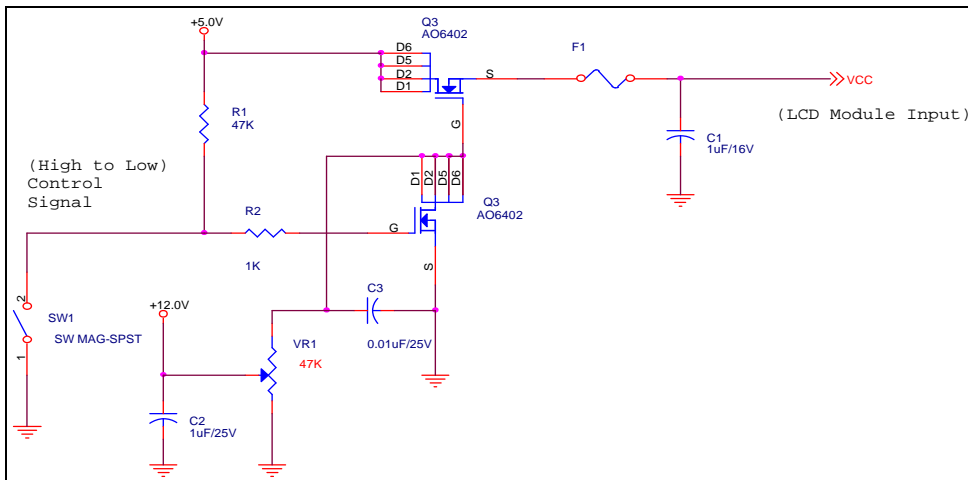
Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Unit	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power		TBD		[Watt]	Note 1/2
IDD	IDD Current		TBD		[mA]	Note 1/2
IRush	Inrush Current		TBD		[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	TBD	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern

Note 3 : Measure Condition



Vin rising time

5.1.2 Signal Electrical Characteristics

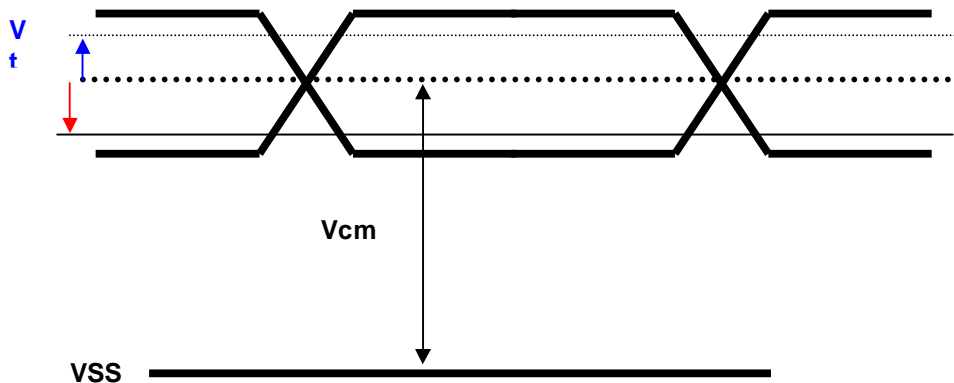
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





5.2 Backlight Unit

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Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Forward Voltage	V_F	2.95	3.0	3.3	[Volt]	($T_a=25^\circ\text{C}$)
LED Forward Current	I_F		20	-	[mA]	($T_a=25^\circ\text{C}$)
LED Power consumption	P_{LED}		-	1.76	[Watt]	($T_a=25^\circ\text{C}$) Note 1
LED Life-Time	N/A	10,000	-	-	Hour	($T_a=25^\circ\text{C}$) $I_F=20\text{ mA}$ Note 2
Output PWM frequency	F_{PWM}	-	200	1K	Hz	
Duty ratio	--	15	--	100	%	

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) x I_F (Normal Distribution) / Efficiency

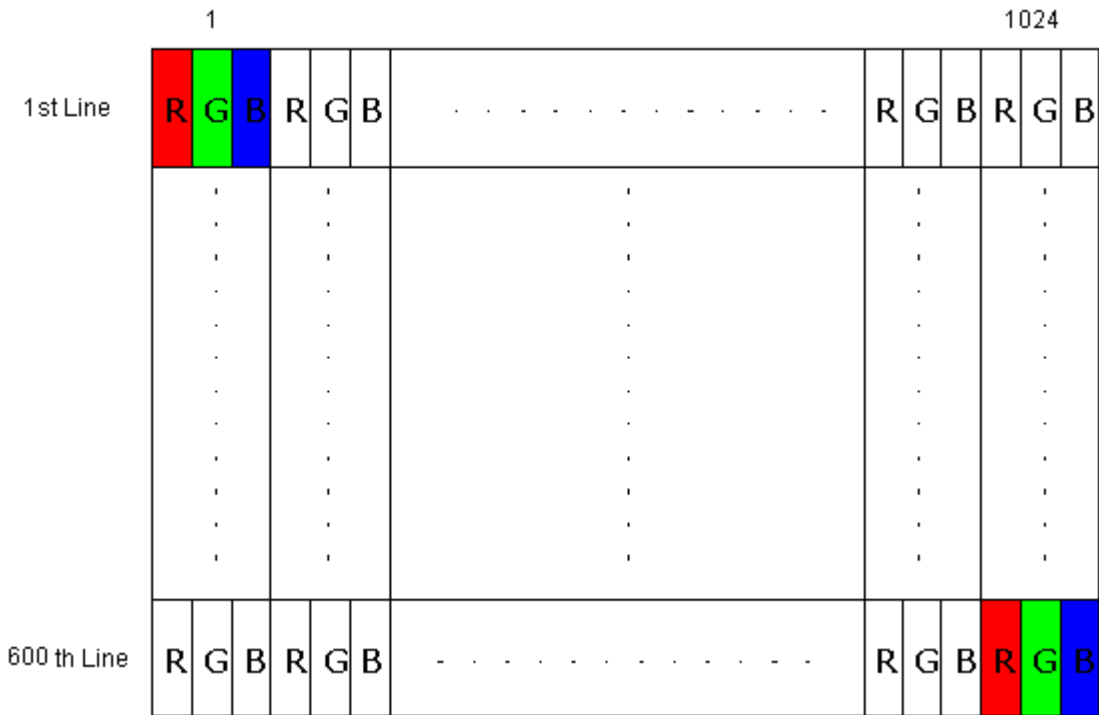
Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 3: This panel will support lower duty ration at PWM conditional frequency. The PWM frequency constrain between 100 Hz to 300 Hz and a same typical 200Hz. The duty ration will support from 5% to 100

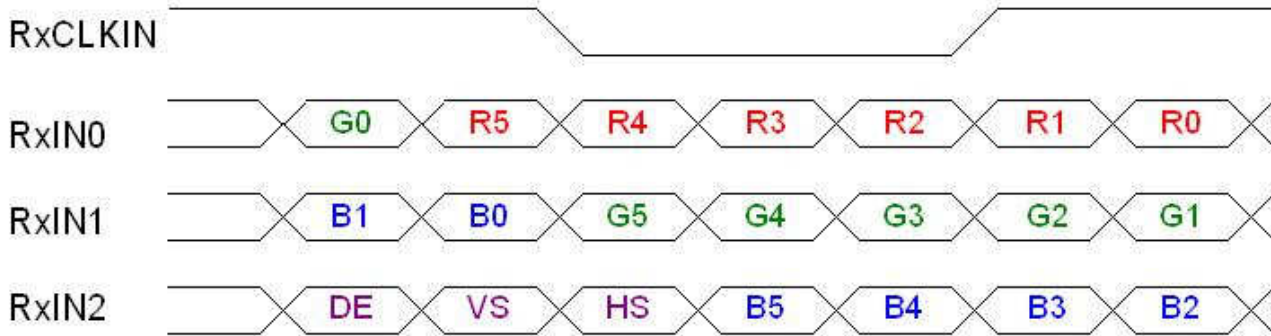
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 54.2MHZ.The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Signal Description/Pin Assignment

Pin	Signal	Description
1	GND	Ground
2	AVDD	PowerSupply,3.3V(typical)
3	AVDD	PowerSupply,3.3V(typical)
4	DVDD	DDC 3.3Vpower
5	AGING	No Connection (Reserve for AUO)
6	SCL	DDCClock
7	SDA	DDCData
8	Rin0-	-LVDSdifferential data input(R0-R5,G0)
9	Rin0+	+LVDSdifferential data input(R0-R5,G0)
10	GND	Ground
11	Rin1-	-LVDSdifferential data input(G1-G5,B0-B1)
12	Rin1+	+LVDSdifferential data input(G1-G5,B0-B1)
13	GND	Ground
14	Rin2-	-LVDSdifferential data input(B2-B5,HS,VS,DE)
15	Rin2+	+LVDSdifferential data input(B2-B5,HS,VS,DE)
16	GND	Ground
17	CIKIN-	-LVDSdifferential clock input
18	CIKIN+	+LVDSdifferential clock input
19	GND	Ground
20	LVDS_EN	LVDS Enable
21	NC	No Connection (Reserve)
22	GND	Ground
23	NC	No Connection (Reserve)
24	NC	No Connection (Reserve)
25	GND	Ground–Shield
26	NC	No Connection (Reserve)
27	NC	No Connection (Reserve)
28	GND	Ground–Shield
29	NC	No Connection (Reserve)
30	NC	No Connection (Reserve)
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)



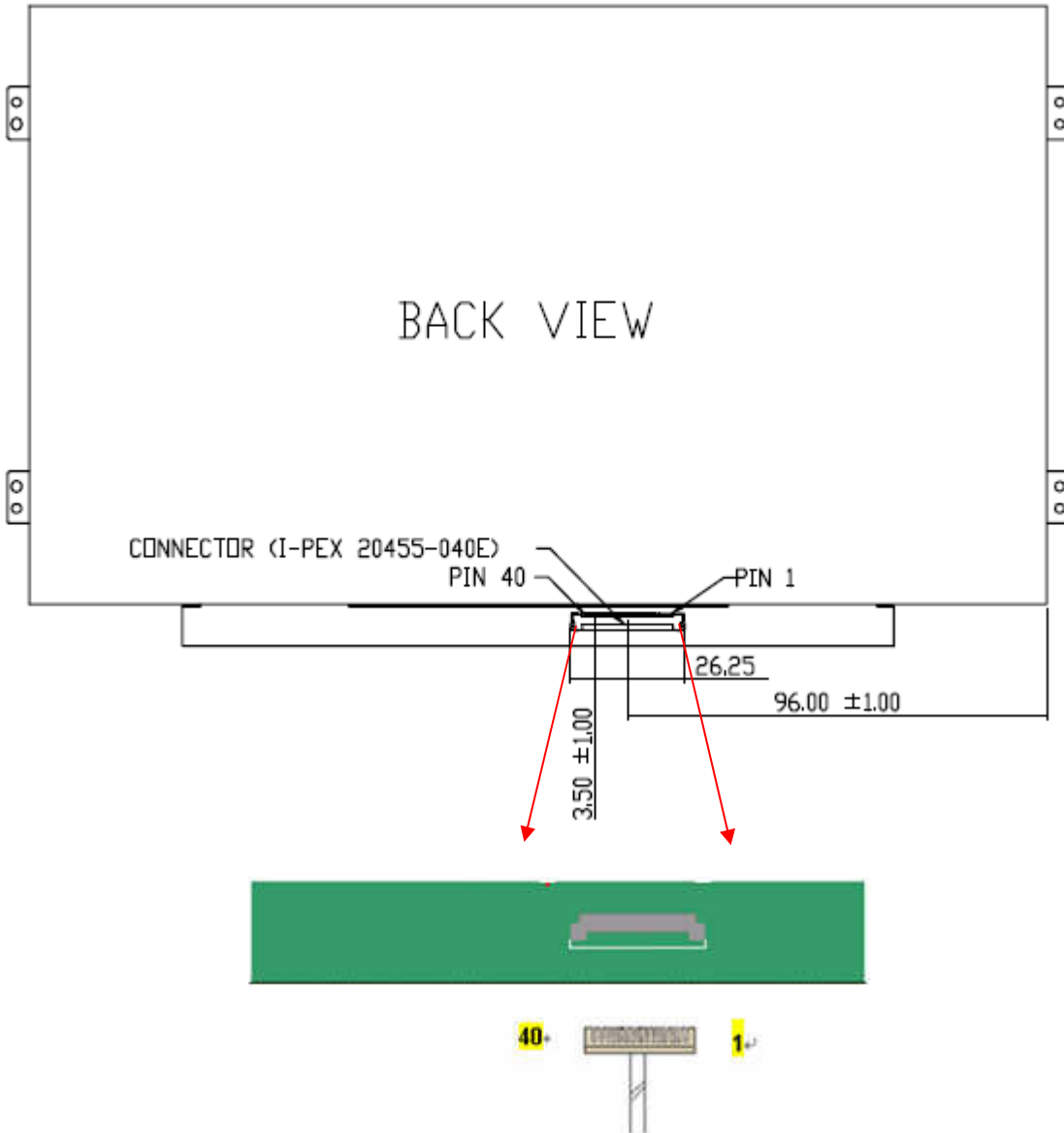
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35	PWM	System PWM Signal Input
36	LED_EN	LED enable pin(+3.3 V Input)
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)
39	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)
40	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)

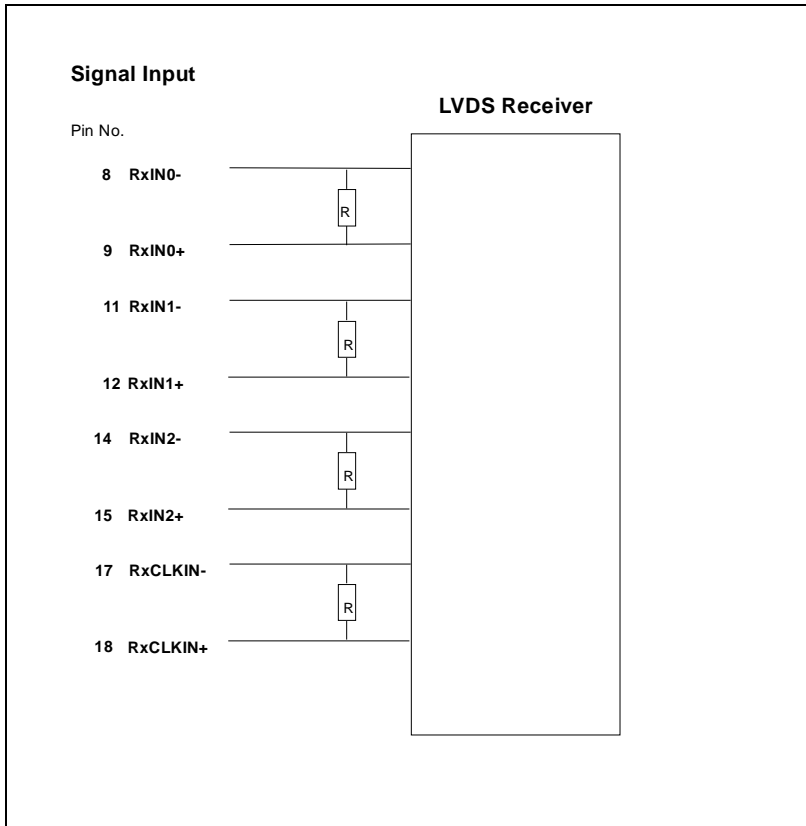
LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Note1.



Note2: Input signals shall be low or High-impedance state when VDD is off.
 internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

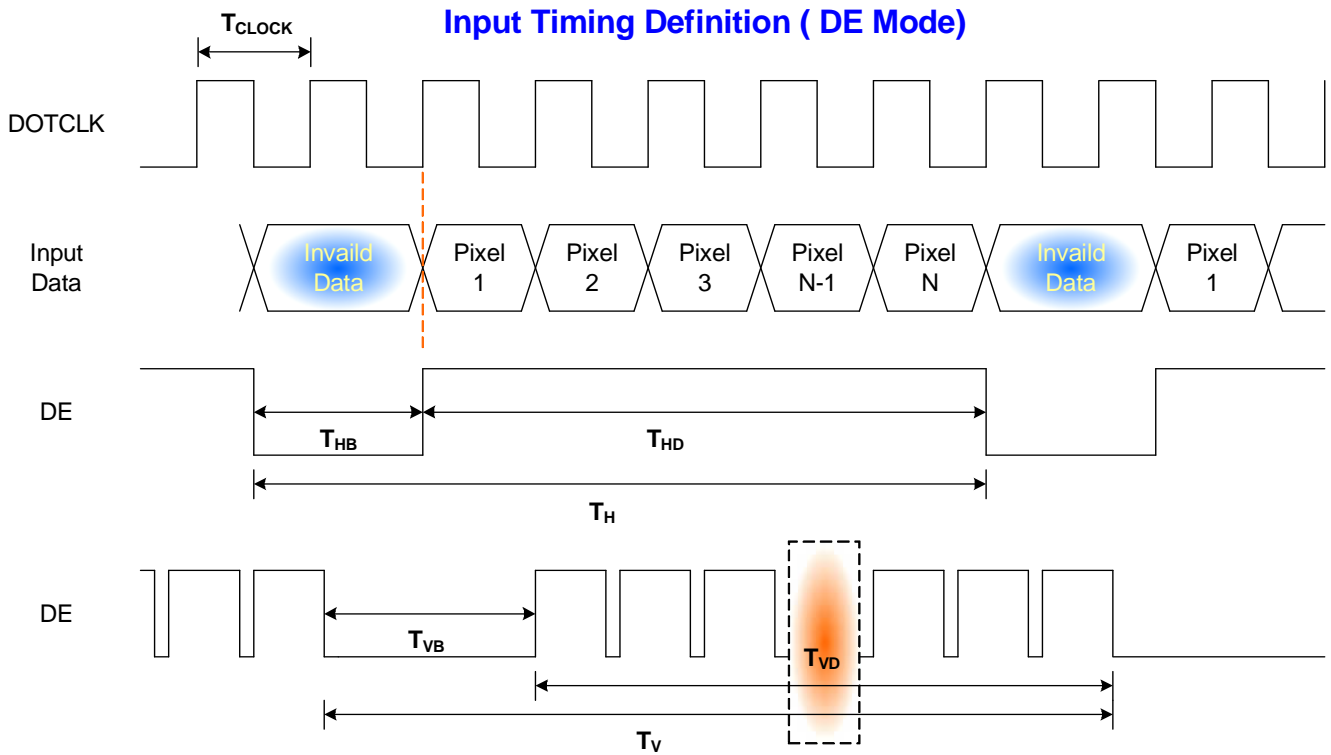
6.4.1 Timing Characteristics

Basically, interface timings should match the 1024 x 600 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frame Rate	-		60		Hz
Clock frequency	$1/T_{\text{Clock}}$		50.4		MHz
Vertical Section	Period	T_V	625		T_{Line}
	Active	T_{VD}	600		
	Blanking	T_{VB}	25		
Horizontal Section	Period	T_H	1344		T_{Clock}
	Active	T_{HD}	1024		
	Blanking	T_{HB}	320		

Note : DE mode only

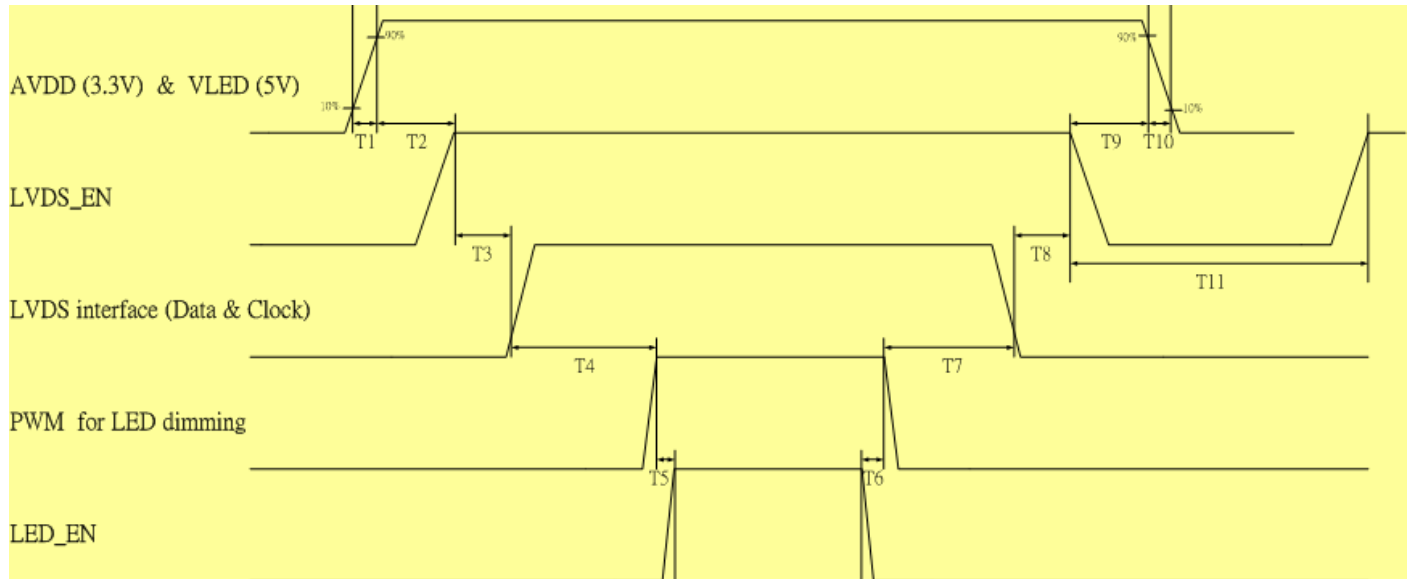
6.4.2 Timing diagram



6.5 Power Sequence

6.5.1 Panel Power Sequence

VDD power and LED on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	10	-	-	ms
T3	30	40	90	ms
T4	200	-	-	ms
T5	10	-	-	ms
T6	0	-	-	ms

Parameter	Value			Unit
	Min.	Typ.	Max.	
T7	110	-	-	ms
T8	0	16	80	ms
T9	>0 (must exceed 0)			ms
T10	-	10	30	ms
T11	1000	-	-	ms



7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12
Mating Housing/Part Number	IPEX 20453-040T-11

8. 8. LED Driving Specification

8.1 Connector Description

It is a integrative interface and comibe into LVDS connector. The type and mating refer to section 7.

8.2 Pin Assignment

31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	PWM	System PWM Signal Input
36	LED_EN	LED enable pin(+3.3V Input)
37	NC	No Connection (Reserve)
38	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)
39	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)
40	VLED	LED Power Supply 5V (Tolerance: +,- 0.5V)



9. Vibration and Shock Test

9.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

9.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

10. Reliability

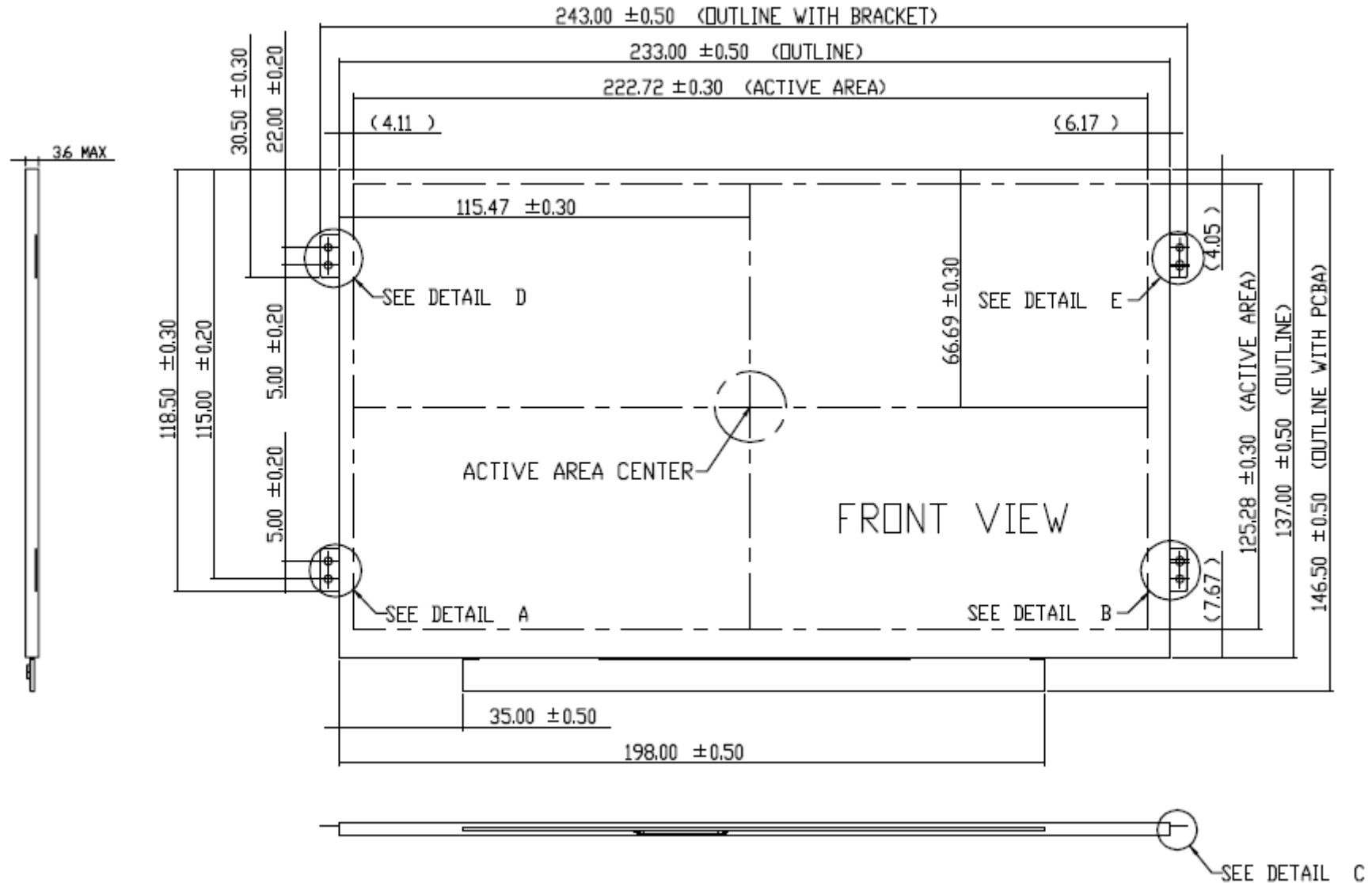
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 35%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ± 15 KV	Note 1

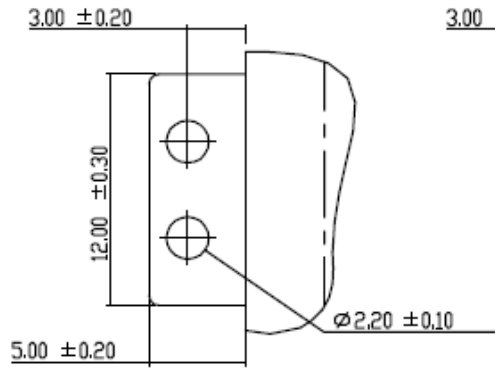
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost
 . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

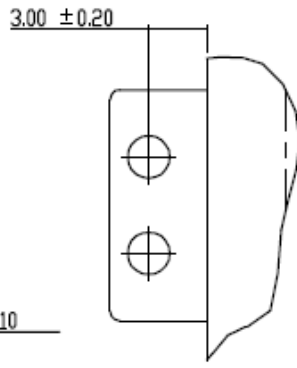
11. Mechanical Characteristics

11.1 LCM Outline Dimension

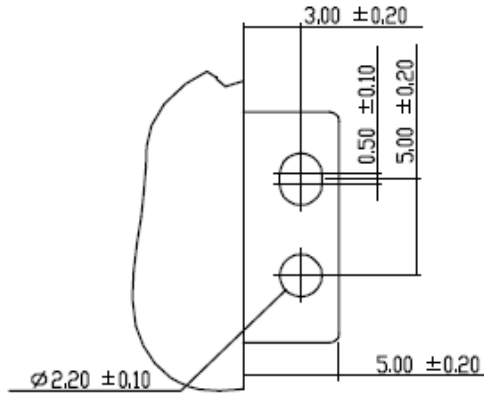




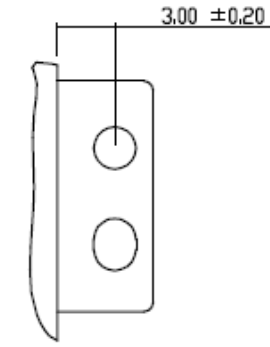
DETAIL A
SCALE 5.000



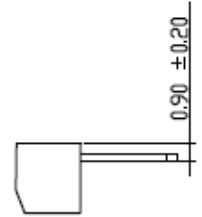
DETAIL D
SCALE 5.000



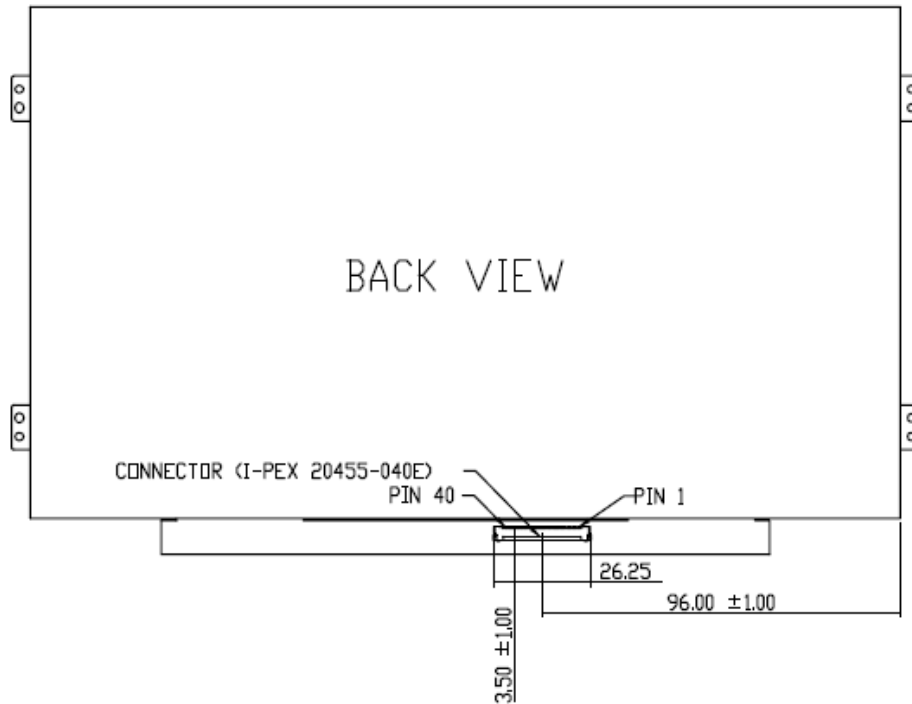
DETAIL B
SCALE 5.000



DETAIL E
SCALE 5.000



DETAIL C
SCALE 5.000



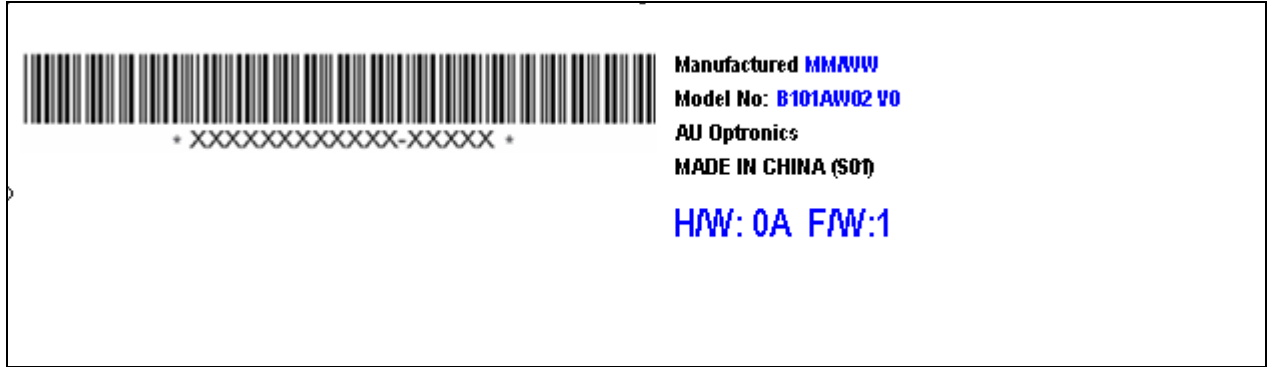


Product Specification

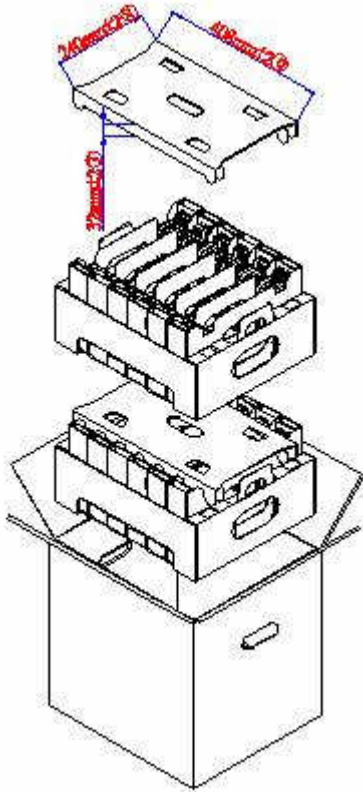
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11. Shipping and Package

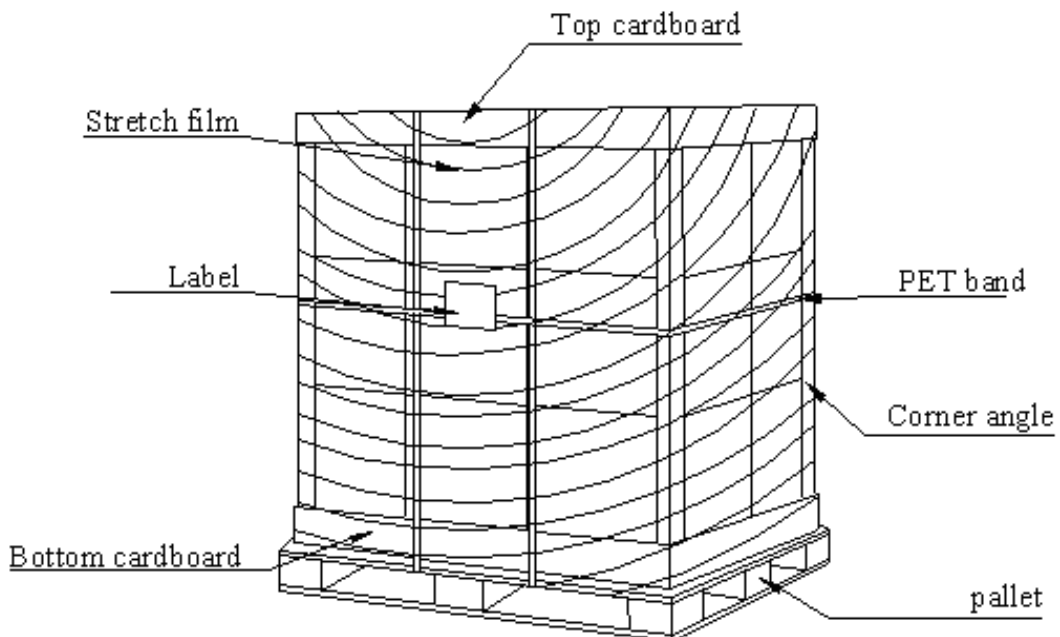
11.1 Shipping Label Format



11.2 Carton package



11.3 Shipping package of palletizing sequence





12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	D2	11010010	210
0B	hex, LSB first	20	00100000	32
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	12	00010010	18
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	03	00000011	3
14	Video input def. (digital I/P, non-TMDS, CRGB)	80	10000000	128
15	Max H image size (rounded to cm)	16	00010110	22
16	Max V image size (rounded to cm)	0D	00001101	13
17	Display Gamma (=gamma*100)-100)	78	01111000	120
18	Feature support (no DPMS, Active OFF, RGB, tmg Blk#1)	0A	00001010	10
19	Red/green low bits (Lower 2:2:2:2 bits)	2B	00101011	43
1A	Blue/white low bits (Lower 2:2:2:2 bits)	69	01101001	105
1B	Red x (Upper 8 bits)	97	10010111	151
1C	Red y/ highER 8 bits	57	01010111	87
1D	Green x	55	01010101	85
1E	Green y	96	10010110	150
1F	Blue x	29	00101001	41
20	Blue y	21	00100001	33
21	White x	4F	01001111	79
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0



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24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	B0	10110000	176
37	Pixel Clock/10000 USB	13	00010011	19
38	Horz active Lower 8bits	00	00000000	0
39	Horz blanking Lower 8bits	40	01000000	64
3A	HorzAct:HorzBlnk Upper 4:4 bits	41	01000001	65
3B	Vertical Active Lower 8bits	58	01011000	88
3C	Vertical Blanking Lower 8bits	19	00011001	25
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	20	00100000	32
3E	HorzSync. Offset	18	00011000	24
3F	HorzSync.Width	88	10001000	136
40	VertSync.Offset : VertSync.Width	31	00110001	49
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	DF	11011111	223
43	Vertical Image Size Lower 8bits	7D	01111101	125
44	Horizontal & Vertical Image Size (upper 4:4 bits)	00	00000000	0
45	Horizontal Border (zero for internal LCD)	00	00000000	0
46	Vertical Border (zero for internal LCD)	00	00000000	0
47	Signal (non-intr, norm, no stereo, sep sync, neg pol)	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0



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4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	30	00110000	48
74	Manufacture P/N	31	00110001	49
75	Manufacture P/N	41	01000001	65
76	Manufacture P/N	57	01010111	87
77	Manufacture P/N	30	00110000	48



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78	Manufacture P/N	32	00110010	50
79	Manufacture P/N	20	00100000	32
7A	Manufacture P/N	56	01010110	86
7B	Manufacture P/N	30	00110000	48
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	C7	11000111	199