

mass integrated

global part distribution • product lifecycle partner
excess inventory management • value-ad service provider



Data sheet provided by Mass Integrated

massintegrated.com • displayalliance.com

Please call +1.978.465.6190
Email: sales@massintegrated.com



ISO 9001: 2008

Mass Integrated complies with all DMCA takedown notices. Please send a formal DMCA Takedown Notice to Mass Integrated Systems, Inc. • 18 Henry Graf Jr. Road, Unit 1 • Newburyport, MA 01950.

SPECIFICATION FOR COLOR STN LCD MODULE

MODEL NO: [TM9664A2KFWG](#)

CUSTOMER:

TIANMA MICROELETRONIC CO., LTD
22/F HANGDU BUILDING, CATIC ZONE,
SHEN NAN ROAD CENTRAL
SHENZHEN, CHINA
TEL: (86-755) 83790774
FAX: (86-755) 83790431
WEB: WWW.TIANMA.COM



PREPARED	CHECKED	VERIFIED BY R&D DEPT	VERIFIED BY QC DEPT	APPROVED

REVISION RECORD

Date	Rev.No.	Revision Items	Prepared	Checked	Approved
2005.10.10	V1.0	First edition	XIONGHenian		

CONTENTS

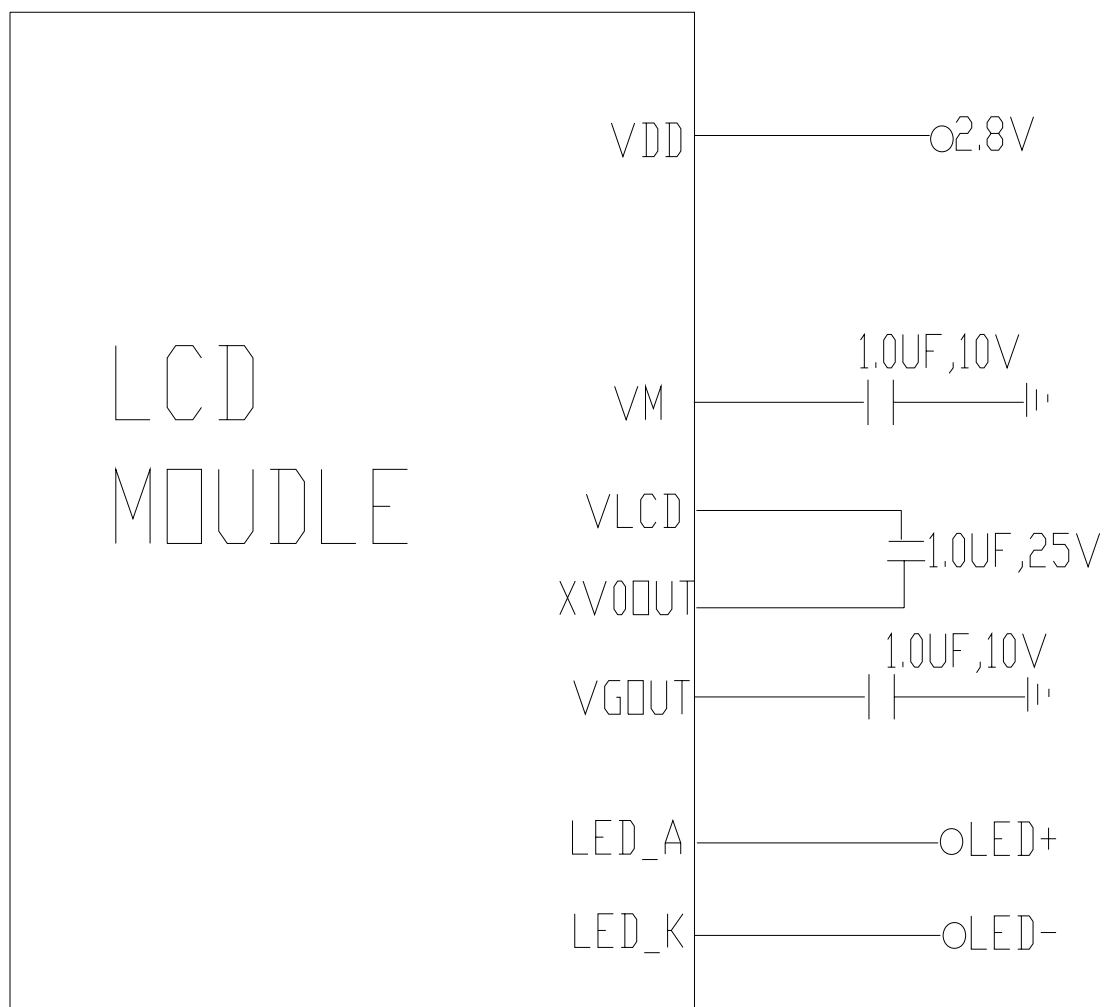
	Page
1.General Specifications -----	3
2. Outline Drawing -----	4
3. Circuit Block Diagram -----	5
4. Absolute Maximum Ratings -----	7
5. Electrical Specifications and Instruction Code -----	8
6. Optical Characteristics -----	17
7. Reliability -----	21
8. Quality level-----	22
9. Precautions for Use of LCD Modules -----	27

1.General Specifications

Item	Contents	Unit	Note
LCD Type	Color STN	-	
Display color	65K	-	1
LCD Duty	1/70	-	
LCD Bias	1/9	-	
Viewing Direction	6:00	O'Clock	
Viewing Area(W×H)	21.55×15.43	mm	
Active Area(W×H)	20.12×13.43	mm	
Number of Dots	96(RGB)×64	mm	
Dot Size(W×H)	0.20×0.20	mm	
Dot Pitch(W×H)	0.21×0.21	mm	
Controller	ST7628	-	
V _{DD}	2.8	V	
V _{op}	9.5	V	
Outline Dimensions	Refer to outline drawing on next page		
Operating Temperature	-20~+70℃	-	
Storage Temperature	-30~+80℃	-	
Weight	2.74	g	
Data transfer	3-wire,4-wire serial bus and 8 bit/4 bit parallel bus(8080 or 6800)		
Polarizer Mode	Transmissive /Negative	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

3.2 POWER SUPPLY Circuit Block



4. Absolute Maximum Ratings(Ta=25°C)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	-0.3	3.0	V	1,2
Power Supply Voltage for LCD	V _{op}	-0.3	18.0	V	
Logic Signal Input Voltage	V _I	-0.3	V _{DD} +0.5	V	
Operating Temperature	T _{op}	-20	+70	°C	
Storage Temperature	T _{st}	-30	+80	°C	

Notes:

If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

2. V_{DD} > V_{SS} must be maintained.

5. Electrical Specifications and Instruction Code

5.1 Electrical characteristics (Ta=25°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Operation voltage	V_{OP}	Ta=25°C	9.2	9.5	9.8	V	1
Input voltage	'H'	V_{IH}	$V_{DD}=2.8V$	$0.8V_{DD}$	-	V_{DD}	V
	'L'	V_{IL}	$V_{DD}=2.8V$	V_{SS}	-	$0.2V_{DD}$	V
Output Voltage	'H'	V_{OH}	-	$0.8V_{DD}$	-	V_{DD}	V
	'L'	V_{OL}	-	V_{SS}	-	$0.2V_{DD}$	V
Current Consumption	I_{CC}	Normal mode	-	-	3	mA	2

Note:

1: IC default setting, Duty:1/70,Bias:1/9.

2: Display full white, exclude backlight.

5.2 LED backlight specification

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Forward voltage	V_f	$I_f=15mA$		3.2		V	
Forward current	Normal	I_{pn}	1-chip	15		mA	
Luminance	L_v	$I_f=15mA$	2600			Cd/m ²	
Average			80%				

5.3 Interface Signals

Pin No.	Symbol	I/O	Function
1	LED_K	P	<i>Power supply for LED(-)</i>
2	LED_A	P	<i>Power supply for LED(+)</i>
3	A0	I	Register select input pin.
4	RW_WR	I	Read/Write select pin
5-12	D0-D7	I/O	<i>8-Bit Data bus</i>
13	E_RD	I	Read/Write select pin
14	RST	I	Reset signal input pin
15	IF1	I	Parallel/Serial data input select input
16	IF2	I	Parallel/Serial data input select input
17	IF3	I	Parallel/Serial data input select input
18	/CS	I	Chip select input pins
19	VDDI		<i>Power supply for logic circuit</i>
20	VSS		Ground
21	VM		<i>The I/O pin of LCD bias supply voltage</i>
22	VDDA		<i>Power supply for LCD</i>
23	VLCD		<i>Positive LCD driver supply voltages</i>
24	XV0OUT		<i>Negative LCD drive supply voltages.</i>
25	VGOUT		<i>Bias LCD driver supply voltages</i>

5.4 Initialization Table

Command Table-1 , /EXT= H , L , or floating														
Hex	Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Ref
(00h)	NOP	0	1	0	0	0	0	0	0	0	0	0	No Operation	9.1.1
(01h)	SWRESET	0	1	0	0	0	0	0	0	0	0	1	Software reset	9.1.2
(04h)	RDDID	0	1	0	0	0	0	0	0	1	0	0	Read Display ID	9.1.3
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	ID1 read (D23-D16)	
-		1	0	1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID2 read (D15-D8)	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	ID3 read (D7-D0)	
(09h)	RDDST	0	1	0	0	0	0	0	1	0	0	1	Read Display Status	9.1.4
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	(D31-D24)	
-		1	0	1	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	(D23-D16)	
-		1	0	1	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	(D15-D8)	
-		1	0	1	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	(D7-D0)	
(0Ah)	RDDPM	0	1	0	0	0	0	0	1	0	1	0	Read Display Power Mode	9.1.5
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	D2	0	0	-	
(0Bh)	RDDMADCTR	0	1	0	0	0	0	0	1	0	1	1	Read Display MADCTR	9.1.6
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	D3	0	0	0	-	
(0Ch)	RDDCOLMOD	0	1	0	0	0	0	0	1	1	0	0	Read Display Pixel Format	9.1.7
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	0	0	0	0	0	D2	D1	D0	-	
(0Dh)	RDDIM	0	1	0	0	0	0	0	1	1	0	1	Read Display Image Mode	9.1.8
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	0	D5	D4	D3	0	0	0	-	
(0Eh)	RDDSM	0	1	0	0	0	0	0	1	1	1	0	Read Display Signal Mode	9.1.9
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	0	0	0	0	0	0	-	
(0Fh)	RDDSDR	0	1	0	0	0	0	0	1	1	1	1	Read Display Self-diagnostic result	9.1.10
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	D7	D6	D5	D4	0	0	0	0	-	

(10h)	SLPIN	0	1	0	0	0	0	1	0	0	0	0	Sleep in & booster off	9.1.11	
(11h)	SLPOUT	0	1	0	0	0	0	1	0	0	0	1	Sleep out & booster on	9.1.12	
(12h)	PTLON	0	1	0	0	0	0	1	0	0	1	0	Partial mode on	9.1.13	
(13h)	NORON	0	1	0	0	0	0	1	0	0	1	1	Partial off (Normal)	9.1.14	
(20h)	INVOFF	0	1	0	0	0	1	0	0	0	0	0	Display inversion off (normal)	9.1.15	
(21h)	INVON	0	1	0	0	0	1	0	0	0	0	1	Display inversion on	9.1.16	
(22h)	APOFF	0	1	0	0	0	1	0	0	0	1	0	All pixel off (Only for test purpose)	9.1.17	
(23h)	APON	0	1	0	0	0	1	0	0	0	1	1	All pixel on (Only for test purpose)	9.1.18	
(25h)	WRCNTR	0	1	0	0	0	1	0	0	1	0	1	Write contrast	9.1.19	
-		1	1	0	0	EV6	EV5	EV4	EV3	EV2	EV1	EV0	EV = 0 to 127		
(28h)	DISPOFF	0	1	0	0	0	1	0	1	0	0	0	Display off	9.1.20	
(29h)	DISPON	0	1	0	0	0	1	0	1	0	0	1	Display on	9.1.21	
(2Ah)	CASET	0	1	0	0	0	1	0	1	0	1	0	Column address set	9.1.22	
		1	1	0	0	XS6	XS5	XS4	XS3	XS2	XS1	XS0	X_ADDR start: $0 \leq XS \leq 61h$		
		1	1	0	0	XE6	XE5	XE4	XE3	XE2	XE1	XE0	X_ADDR end: $XS \leq XE \leq 61h$		
(2Bh)	RASET	0	1	0	0	0	1	0	1	0	1	1	Row address set	9.1.23	
		1	1	0	0	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y_ADDR start: $0 \leq YS \leq 45h$		
		1	1	0	0	YE6	YE5	YE4	YE3	YE2	YE1	YE0	Y_ADDR end: $YS \leq YE \leq 45h$		
(2Ch)	RAMWR	0	1	0	0	0	1	0	1	1	0	0	Memory write	9.1.24	
		1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data	
(2Dh)	RGBSET	0	1	0	0	0	1	0	1	1	0	1	Color set for 256 or 4k color display	9.1.25	
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (00000)		
-		1	1	0	:	:	:	:	:	:	:	:	:-		
-		1	1	0	-	-	R5	R4	R3	R2	R1	R0	Red tone (11111)		
-		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (000000)		
		1	1	0	:	:	:	:	:	:	:	:	:-		
		1	1	0	-	-	G5	G4	G3	G2	G1	G0	Green tone (111111)		
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (00000)		
		1	1	0	:	:	:	:	:	:	:	:	:-		
		1	1	0	-	-	B5	B4	B3	B2	B1	B0	Blue tone (11111)		
(30h)	PTLAR	0	1	0	0	0	1	1	0	0	0	0	Partial start/end address set	9.1.26	
-		1	1	0	0	PS6	PS5	PS4	PS3	PS2	PS1	PS0	Start address (0~69)		
-		1	1	0	0	PE6	PE5	PE4	PE3	PE2	PE1	PE0	End address (0~69)		

(33h)	SCRLAR	0	1	0	0	0	1	1	0	0	1	1	Scroll Area	9.1.27
-		1	1	0	0	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	TFA= 0~70	
-		1	1	0	0	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	VSA= 0~70	
-		1	1	0	0	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	BFA= 0~70	
(34h)	TEOFF	0	1	0	0	0	1	1	0	1	0	0	Tearing effect line off	9.1.28
(35h)	TEON	0	1	0	0	0	1	1	0	1	0	1	Tearing effect mode set & on	9.1.29
-		1	1	0	-	-	-	-	-	-	-	M	"0": mode1, "1": mode2	
(36h)	MADCTR	0	1	0	0	0	1	1	0	1	1	0	Memory data access control	9.1.30
-		1	1	0	MY	MX	MV	ML	RGB	-	-	-	-	
(37h)	VSCSAD	0	1	0	0	0	1	1	0	1	1	1	Scroll start address of RAM	9.1.31
		1	1	0	0	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	SSA = 0~69	
(38h)	IDMOFF	0	1	0	0	0	1	1	1	0	0	0	Idle mode off	9.1.32
(39h)	IDMON	0	1	0	0	0	1	1	1	0	0	1	Idle mode on	9.1.33
(3Ah)	COLMOD	0	1	0	0	0	1	1	1	0	1	0	Interface pixel format	9.1.34
-		1	1	0	-	-	-	-	-	P2	P1	P0	Interface format	
(DAh)	RDID1	0	1	0	1	1	0	1	1	0	1	0	Read ID1	9.1.35
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	(D7-D0)	
(DBh)	RDID2	0	1	0	1	1	0	1	1	0	1	1	Read ID2	9.1.36
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	(D7-D0)	
(DCh)	RDID3	0	1	0	1	1	0	1	1	1	0	0	Read ID3	9.1.37
-		1	0	1	-	-	-	-	-	-	-	-	Dummy read	
-		1	0	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	(D7-D0)	

Note 1: When /EXT connects to H or floating, commands which are not defined in "Command Table-1" are treated as NOP (00H) command.

Note 2: Commands 10H, 12H, 13H, 20H, 21H, 25H, 28H, 29H, 30H, 36H (Bit ML only), 38H and 39H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects.

During Sleep In mode, these commands are updated immediately.

Read status (09H), Read Display Power Mode (0AH), Read Display MADCTR (0BH), Read Display Pixel Format (0CH), Read Display Image Mode (0DH), Read Display Signal Mode (0EH) and Read Display Self Diagnostic Result (0FH) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.5 Interface Timing Chart

Note: Please refer to UltraChip's UC1681S data sheet for more details.

11.1 Parallel Interface Characteristics bus (8080-series MCU)

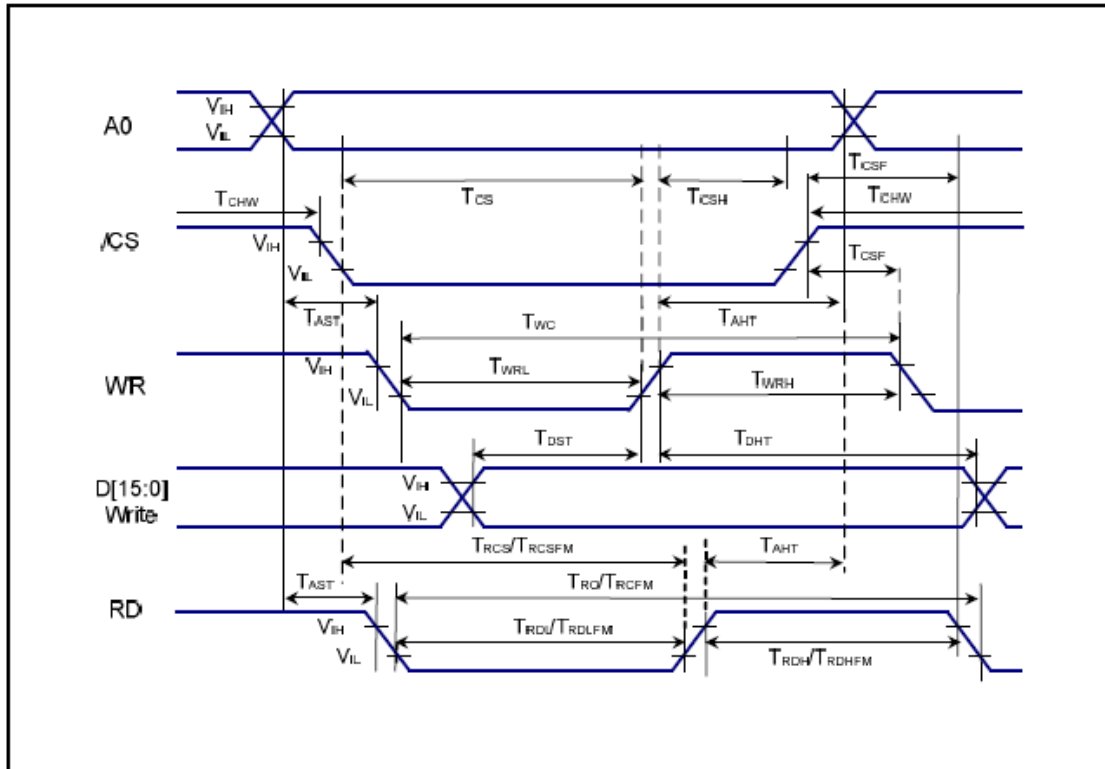


Figure 11.1 Parallel Interface Characteristics bus(8080-series MCU)

(VSS=0V, VDDI=1.65V to 3.0V, VDVA=2.4V to 3.3V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T _{AST}	Address setup time	10	-	ns	-
	T _{AHT}	Address hold time (Write/Read)	10	-	ns	
/CS	T _{CHW}	Chip select "H" pulse width	0	-	ns	
	T _{CS}	Chip select setup time (Write)	35	-	ns	
	T _{RCS}	Chip select setup time (Read ID)	100	-	ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T _{CSF}	Chip select wait time (Write/Read)	10	-	ns	
WR	T _{WC}	Write cycle	250	-	ns	
	T _{WRH}	Control pulse "H" duration	150	-	ns	
	T _{WRL}	Control pulse "L" duration	60	-	ns	
RD (ID)	T _{RC}	Read cycle (ID)	160	-	ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	45	-	ns	
	T _{RDL}	Control pulse "L" duration (ID)	100	-	ns	
RD (FM)	T _{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	355	-	ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	90	-	ns	
D[15:0]	T _{DST}	Data setup time	30	-	ns	
	T _{DHT}	Data hold time	10	-	ns	

11.2 Parallel Interface Characteristics bus (6800-series MCU)

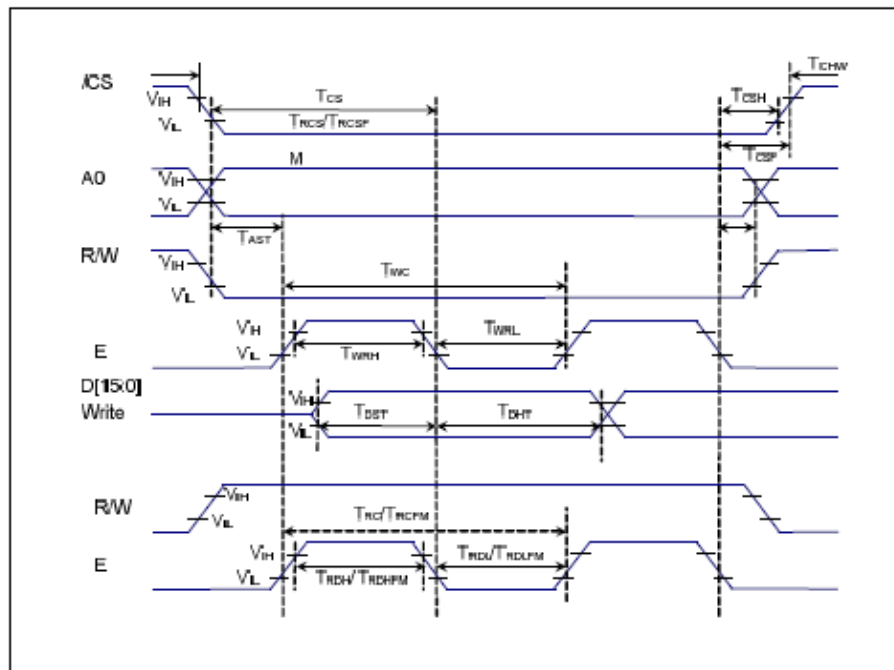


Figure 11.5 Parallel Interface characteristics (6800-Series MCU)

(VSS=0V, VDDI=1.65V to 3.0V, VDPA=2.4V to 3.3V, Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
A0	T _{AST}	Address setup time	10	-	ns	-
	T _{AHT}	Address hold time (Write/Read)	10	-	ns	
/CS	T _{CEW}	Chip select "H" pulse width	0	-	ns	
	T _{CS}	Chip select setup time (Write)	35	-	ns	
	T _{RCS}	Chip select setup time (Read ID)	70	-	ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355	-	ns	
	T _{CSF}	Chip select wait time (Write/Read)	10	-	ns	
	T _{CSH}	Chip select hold time	10	-	ns	
	T _{WC}	Write cycle	250	-	ns	
R/W	T _{WRH}	Control pulse "H" duration	50	-	ns	
	T _{WRL}	Control pulse "L" duration	130	-	ns	
	T _{RC}	Read cycle (ID)	140	-	ns	
E (ID)	T _{RDH}	Control pulse "H" duration (ID)	50	-	ns	When read ID data
	T _{RDL}	Control pulse "L" duration (ID)	20	-	ns	
E (FM)	T _{RCFM}	Read cycle (FM)	400	-	ns	When read from frame memory
	T _{RDHF}	Control pulse "H" duration (FM)	80	-	ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	200	-	ns	
D[15:0]	T _{DST}	Data setup time	10	-	ns	
	T _{DHT}	Data hold time	10	-	ns	

11.3 Serial Interface Characteristics (3-pin Serial)

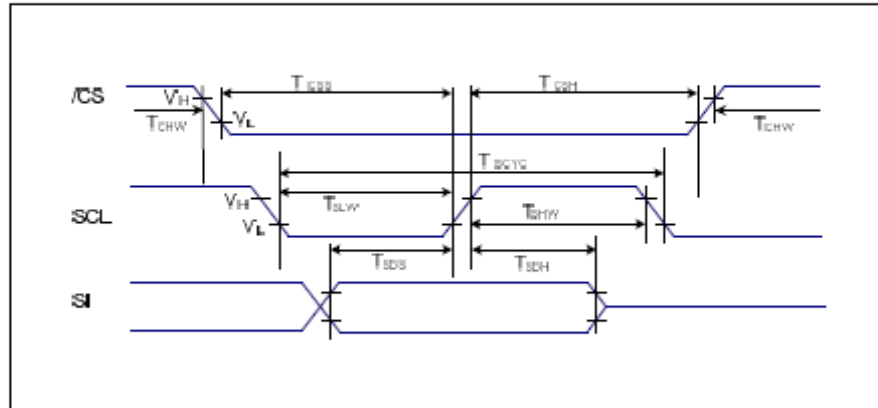


Figure 11.6 3-pin Serial Interface Characteristics

(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V, T_a = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T _{CHW}	/CS "H" pulse width	45		ns	
	T _{CSS}	/CS-SCL setup time(Write)	60		ns	
	T _{CSH}	/CS-SCL hold time(Write)	65		ns	
SCL	T _{SCYC}	Serial clock cycle (Write)	100		ns	
	T _{SHW}	SCL "H" pulse width (Write)	35		ns	
	T _{SLW}	SCL "L" pulse width (Write)	35		ns	
	T _{SCYC}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SI	T _{SDS}	Data setup time	60		ns	
	T _{SDH}	Data hold time	60		ns	

11.4 Serial Interface Characteristics (4-pin Serial)

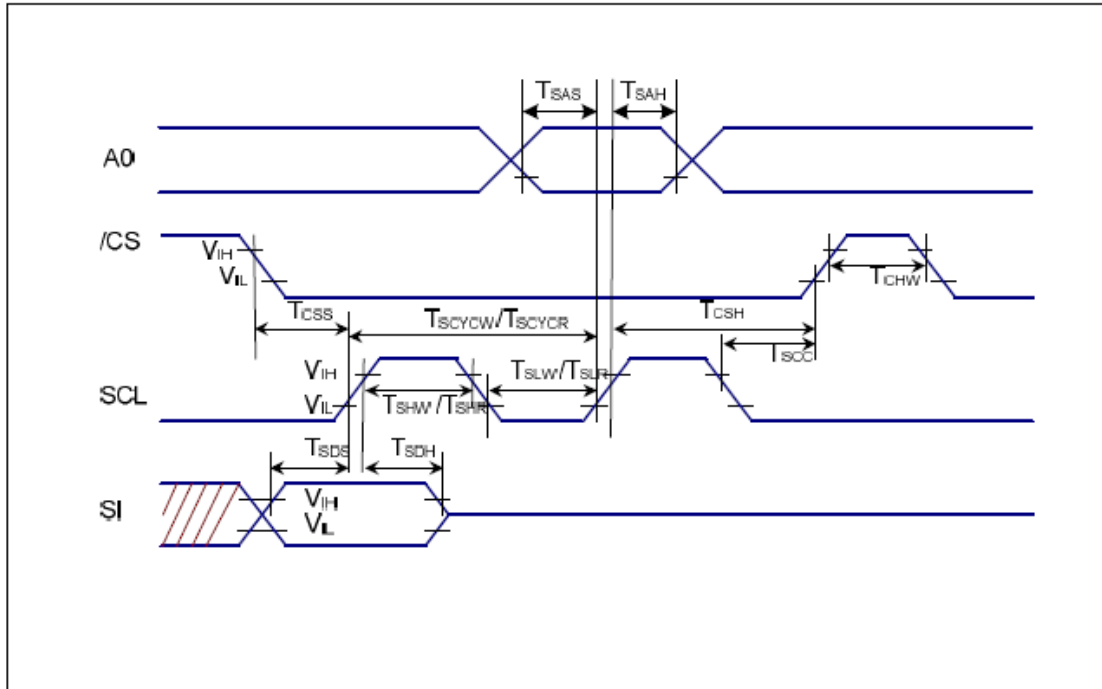


Figure 11.7 4-pin Serial Interface Characteristics

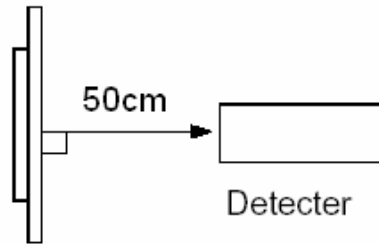
(V_{SS}=0V, V_{DDI}=1.65V to 3.0V, V_{DDA}=2.4V to 3.3V, T_a = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
/CS	T _{CSS}	Chip select setup time	60		ns	
	T _{CSH}	Chip select hold time	65		ns	
	T _{SCC}	Chip select setup time	20		ns	
	T _{CHW}	Chip select pulse width	45		ns	
A0	T _{SAS}	Address setup time	30		ns	
	T _{SAH}	Address hold time	30		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	100		ns	
	T _{SHW}	SCL "H" pulse width (Write)	35		ns	
	T _{SLW}	SCL "L" pulse width (Write)	35		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SI	T _{SDS}	Data setup time	60		ns	
	T _{SDH}	Data hold time	60		ns	

6 Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp	$\Phi_1=0^\circ$	80		200	Cd/m ²	1
Uniformity	ΔBp	$\Phi_2=0^\circ$	70%				1,2
Viewing Angle	Φ_1 (up down)	Cr \geq 2	-40~+35			Deg	3
	Φ_2 (left right)		-30~+30				
Contrast Ratio	Cr	$\Phi_1=0^\circ$ $\Phi_2=0^\circ$	30	40	60	-	4
Response Time	Tr		-	-	180	ms	5
	Tf		70	-	90		
NTSC Ratio	S			25%			

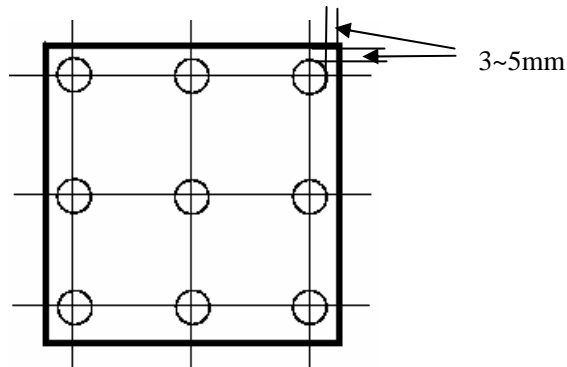
Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ10mm)



Note 2: $\Delta B_p = B_p (\text{Min.}) / B_p (\text{Max.}) \times 100 (\%)$

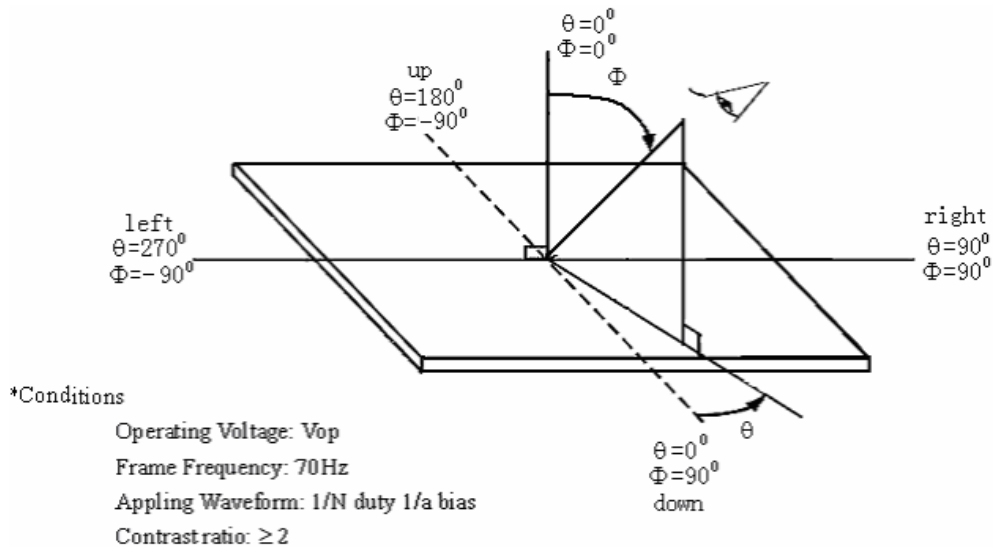
$B_p (\text{Max.})$ = Maximum brightness in 9 measured spots

$B_p (\text{Min.})$ = Minimum brightness in 9 measured spots.

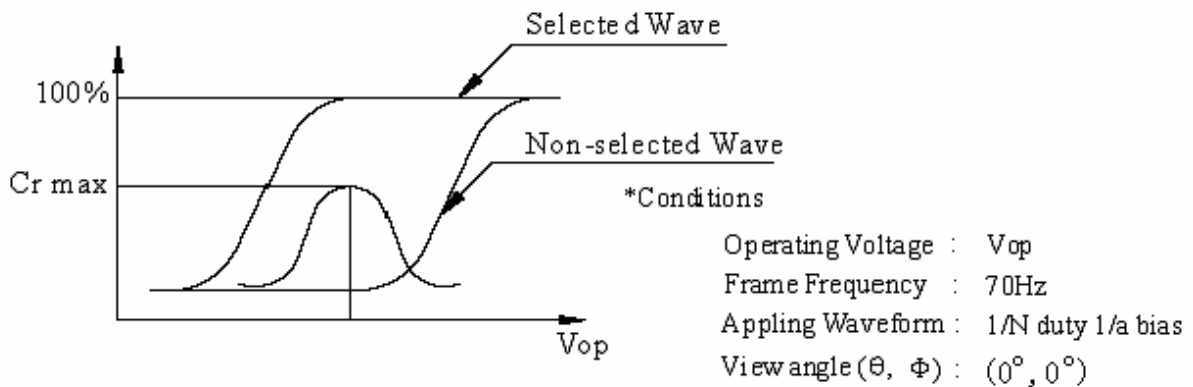


Measurement equipment PR-705 (Φ10mm)

Note 3: Definition of Viewing Angle(Test LCD using DMS501)

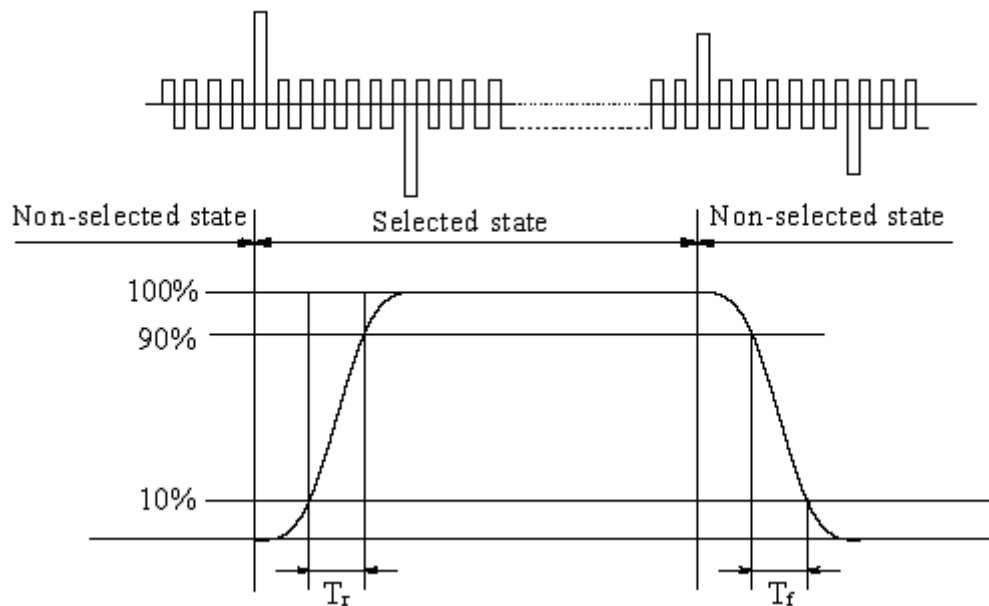


Note 4: Definition of contrast ratio.(Test LCD using DMS501)



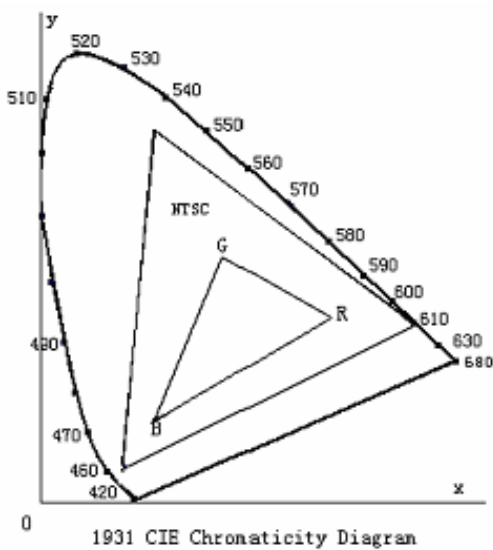
$$\text{Contrast ratio}(Cr) = \frac{\text{Brightness of selected dots}}{\text{Brightness of non-selected dots}}$$

Note 5: Definition of Response time(Test LCD using DMS501)



Operating Voltage: V_{op}
 Frame Frequency: 70Hz
 Applying Waveform: 1/N duty 1/a bias
 View angle (θ, Φ): $(0^\circ, 0^\circ)$

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Color gamut:

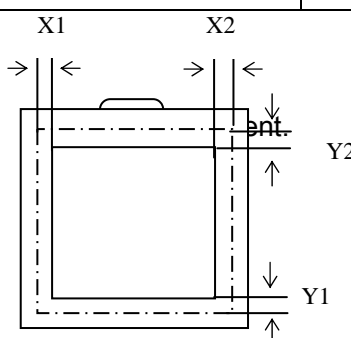
$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

7. Reliability

No.	Test Item	Test condition	Criterion
1	High Temperature Storage	80°C±2°C 96H Restore 4H at 25°C	1. After testing, cosmetic defects should not happen. 2. Total current consumption should not be over 10% of initial value.
2	Low Temperature Storage	-30°C±2°C 96H Restore 4H at 25°C	
3	High Temperature Operation	70°C±2°C 48H Restore 4H at 25°C	
4	Low Temperature Operation	-20°C±2°C 48H Restore 4H at 25°C	
5	High Temperature /Humidity Storage	40°C±2°C 90%RH 48H	
6	Temperature Cycle	-30°C ↔ 25°C ↔ 80°C 5min 30min ↔ 25°C , 5min after 10cycle, Restore 4H at 25°C	
7	Vibration Test (package state)	10Hz~150Hz, 100m/s ² , 120min	Not allowed cosmetic and electrical defects.
8	Shock Test (package state)	Half- sine wave, 300m/s ² , 18ms	
9	Atmospheric Pressure Test	25kPa 16H Restore 2H	

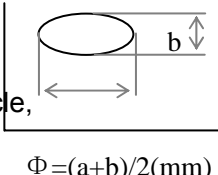
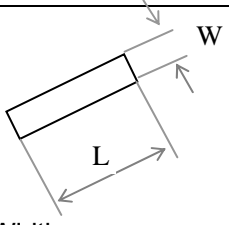
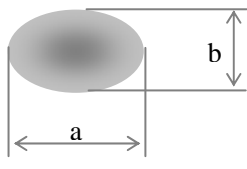
8 Quality level

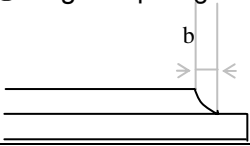
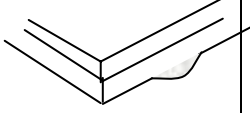
8.1 Notes for quality standard

	Note	
General	Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and Tianma. Viewing Area should be the area which Tianma guarantees. Limited sample should be prior to this Inspection standard. Viewing Judgement should be under static pattern. Inspection conditions Inspection distance : 250 mm (from the sample) Temperature : 25±5°C Inspection angle : 45degrees in LCD view direction	
Definitions of Inspection items	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon dose not change with voltage.
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage.
	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass.
	Glass defect	Glass crack, Shaved corner of glass, Surplus glass
Definitions of Inspection ranges	 <p>Dividing A zone and B zone proceed to</p> <p>A zone : Inside Viewing area B zone : Outside Viewing area X1(A.A~V.A): mm X2(A.A~V.A): mm Y1(A.A~V.A): mm Y2(A.A~V.A): mm</p>	

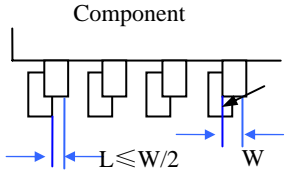
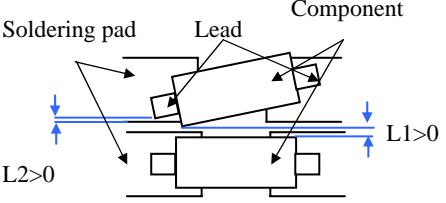
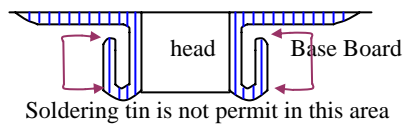
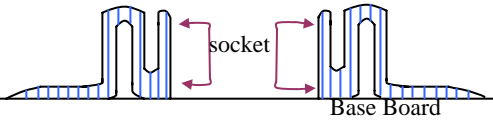
Outgoing Inspection standard	Inspection level II Normal Inspection Sampling standard conforms to GB2828	
	Rank	Inspection Item
	Major defect	All Functional defects(Such as No display, Display abnormally, Open or missing segment, Short circuit, Missing component, No sound, Blight abnormally),Outline dimension beyond the drawing
Minor defect	Appearance defects, such as Black/White spot, Bright spot, Pinhole, Black/White line, Contrast variation, Bubble Glass defect, Polarizer defect, and so on. Details of the standard as follows.	AQL(Number of defective LCMs counted)
		0.65
		1.50

8.2 Standards of inspection items

Inspection item	Judgement standard			
	Category	Acceptable number		
		A zone	B zone	
1 Black spot, White spot, Bright Spot, Pinhole Foreign Particle, Bubble and Particle Between polarizer and glass, Scratch on polarizer  $\Phi = (a+b)/2(\text{mm})$	A	$\Phi \leq 0.15$	Neglect	Neglected
	B	$0.15 < \Phi \leq 0.20$		
	C	$0.20 < \Phi \leq 0.30$	2	
	D	$0.30 < \Phi$	1	
			0	
	Total defective point(B,C)		3	
2 Black line, White line, Bubble and Particle Between Polarizer and glass, Scratch on polarizer  W:Width, L:Length(mm)	A	$W \leq 0.10$	Neglected	Neglected
	B	$0.01 < W \leq 0.03 \quad L \leq 3.0$		
	C	$0.03 < W \leq 0.05 \quad L \leq 3.0$	2	
	D	$0.05 < W$	1	
			0	
	Total defective point(B,C)		2	
3 Contrast variation  $\Phi = (a+b)/2(\text{mm})$	A	$\Phi \leq 0.2$	Neglected	Neglecte
	B	$0.2 < \Phi \leq 0.3$		
	C	$0.3 < \Phi \leq 0.4$	2	d
	D	$0.4 < \Phi$	1	
			0	
	Total defective point(B,C)		3	
4 Bubble inside cell		any size	none	none
5 Polarizer defect (if Polarizer is used)	Scratch and damage on polarizer, Particle on polarizer or between polarizer and glass.	Refer to item 1 and item 2.		

		Bubble, dent and convex	<table border="1"> <tbody> <tr> <td>A</td> <td>$\Phi \leq 0.3$</td> <td>Neglected</td> <td>Neglecte</td> </tr> <tr> <td>B</td> <td>$0.3 < \Phi \leq 0.7$</td> <td>2</td> <td>d</td> </tr> <tr> <td>C</td> <td>$0.7 < \Phi$</td> <td>0</td> <td></td> </tr> <tr> <td colspan="2">Total defective point(B,C)</td> <td>2</td> <td></td> </tr> </tbody> </table>	A	$\Phi \leq 0.3$	Neglected	Neglecte	B	$0.3 < \Phi \leq 0.7$	2	d	C	$0.7 < \Phi$	0		Total defective point(B,C)		2	
A	$\Phi \leq 0.3$	Neglected	Neglecte																
B	$0.3 < \Phi \leq 0.7$	2	d																
C	$0.7 < \Phi$	0																	
Total defective point(B,C)		2																	
6	Surplus glass	① Stage surplus glass 	$b \leq 0.3\text{mm}$																
		② Surrounding surplus glass 	Should not influence outline dimension and assembling.																

Inspection item		Judgment standard									
		Category(application: B zone)									
7	Glass defect crack	①The front of lead terminals	<table border="1"> <tr> <td>A</td> <td>If $a \leq t$ and $b \leq 1.0$, c is not limited</td> </tr> <tr> <td>B</td> <td>$a \leq t$, $1 \leq b \leq 2\text{mm}$, $c \leq 3\text{mm}$</td> </tr> <tr> <td>C</td> <td>If glass crack cover alignment mark, $b \leq 0.5\text{mm}$.</td> </tr> <tr> <td>D</td> <td>Crack at two sides of lead terminals should not cover patterns and alignment mark</td> </tr> </table>	A	If $a \leq t$ and $b \leq 1.0$, c is not limited	B	$a \leq t$, $1 \leq b \leq 2\text{mm}$, $c \leq 3\text{mm}$	C	If glass crack cover alignment mark, $b \leq 0.5\text{mm}$.	D	Crack at two sides of lead terminals should not cover patterns and alignment mark
		A	If $a \leq t$ and $b \leq 1.0$, c is not limited								
		B	$a \leq t$, $1 \leq b \leq 2\text{mm}$, $c \leq 3\text{mm}$								
		C	If glass crack cover alignment mark, $b \leq 0.5\text{mm}$.								
D	Crack at two sides of lead terminals should not cover patterns and alignment mark										
②Surrounding crack—non-contact side	$b < \text{Inner border line of the seal}$										
③ Surrounding crack— contact side	$b < \text{Outer border line of the seal}$										
④Corner	<table border="1"> <tr> <td>A</td> <td>$a \leq t$, $b \leq 3.0$, $c \leq 3.0$</td> </tr> </table> <p>*Glass crack should not cover patterns used for</p>	A	$a \leq t$, $b \leq 3.0$, $c \leq 3.0$								
A	$a \leq t$, $b \leq 3.0$, $c \leq 3.0$										

Inspection item		Judgement standard	
8	PCB defect	<p>Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/2 width of the pin (Pic.1); the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted (Pic.2)</p>	 <p>Component</p> <p>$L \leq W/2$</p> <p>W</p>  <p>Soldering pad</p> <p>Lead</p> <p>Component</p> <p>$L1 > 0$</p> <p>$L2 > 0$</p>
		<p>lead defect: The lead lack must be less than 1/2 of its width; The lead burr must be less than 1/2 of the seam; Impurities connect with the near leads is not permitted</p>	
		<p>Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted</p>	 <p>head</p> <p>Base Board</p> <p>Soldering tin is not permit in this area</p>  <p>socket</p> <p>Base Board</p> <p>Soldering tin is not permit in this area</p>

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer.

Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : $0^{\circ}\text{C} \sim 40^{\circ}\text{C}$

Relatively humidity: $\leq 80\%$

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.